Abstract— Increasing the ADC speed without using exotic and expensive technologies and without losing too much in resolution, became possible by time interleaving ADC method. Unfortunately, the performance of Time-Interleaved ADC (TIADC) is sensitive to offset, gain and nonlinearity mismatch as well as timing errors between interleaved channels. These errors cause distortion in the sampled signal. In this paper we will summarize the offset, gain and timing errors mismatch effects largely coated in literature. First, a SIMULINK floating point model was developed to validate these formulas. As we have to develop some digital algorithms to compensate these errors, we have focus on another modeling methodology using VHDL-AMS, [12]. This paper presents, a comparison between these to approaches in term of flexibility, arithmetic precision and speed computation.

I. INTRODUCTION

To achieve high enough sample rates, an array of M interleaved ADCs can be used. The TIADC system works as follow:

![TIADC Structure](image)

**Fig. 1** Time interleaved ADC structure

It consists of M ADC’s in parallel, an analog demultiplexer at the input, and a digital multiplexer at the output. Each ADC operates at the overall sampling rate divided by M. During operation, the analog demultiplexer selects each ADC in turn to process the input signal. The corresponding digital multiplexer selects the digital output of each ADC periodically and forms a high-speed ADC output. With interleaving, the overall sampling rate is M times higher than the sampling rate of the ADC in each channel. The required die area and power dissipation have also increased, [4] and [5].

In previous works [3], we were interested to model this structure. A Simulink floating-point model was developed. The goal consist on verifying the mathematical formulas of the gain, offset, and timing mismatch. We suppose that some errors does not exist and we make only one of them changed. A spectrum of output signal is drawn, and we verify the localization of non harmonic component due to the appropriate mismatch. The results was sufficient in gain and offset mismatch. For the timing error mismatch, the Simulink model shows some limits with high frequency. In the jitter model we have to insert a large value of jitter taking into account the internal jitter and the test bench one. The interest of using VHDL-AMS description is to dissociate these two jitters during the modeling process.

As future work, we will implement in DSP some algorithms to detect and compensate the mismatch error. We are interesting to two TIADC channel, because it cover a wide range of application. Before implementing the DSP, we have to prepare a material environment which consist on modeling the ADC (S/H, quantizer and saturation bloc) with all static errors (offset, gain and nonlinearity) and timing errors using both SIMULINK and VHDL-AMS.

In the second section we develop all theoretical formulas about offset, gain and timing errors in temporal and frequency domain. Taking in account this formulas, we will develop the SIMULINK model of two ADC channels. Spectral and histogram analyses validate the mathematical formulas. In the same way, the fourth section presents a new model using VHDL-AMS description. The last section gives advantages and drawbacks of these two modeling approaches.

II. INDIVIDUAL CHANNEL MISMATCH

Extensive work has been done to estimate the effects of offset, gain, and aperture mismatches in time-interleaved
ADC’s [4]-[10]. For simplicity reasons, we will take the example of two ADCs to express mismatch effects. This assumption is not false, since interleaving two ADCs cover a large domain of application. It is more coherent to evaluate theoretically the individual channel mismatch effects of two ADCs. Hereafter, we will use following notations: f_0 and ω_0 are respectively the input frequency and pulsation. T and f_s are respectively the sampling period and frequency. V_{os1} and V_{os2} are the offsets of each channel. G_1 and G_2 are the gain of the first and the second channel. The ADC resolution in simulations is set to 8.

**A. Offset mismatch effects**

Different offsets in ADC channels contribute to a dc value as well as a periodic additive pattern in the output of the ADC array. A mathematical analysis of the output of a two-channel time-interleaved ADC with only offset error is given here. Let us consider the two ADC interleaved system fed by sinusoidal input \( x(t) = \cos(\omega_0 t + \phi) \). The ADC output can be written as follow:

\[
y[n] = \cos(\omega_0 nT + \phi) + V_{os1}, \quad n = \text{even} \tag{1}
\]

\[
y[n] = \cos(\omega_0 nT + \phi) + V_{os2}, \quad n = \text{odd} \tag{2}
\]

Let \( V_{os} = 0.5(V_{os1} + V_{os2}) \) and \( \Delta V_{os} = V_{os1} - V_{os2} \), then the output can be written as

\[
y[n] = \cos(\omega_0 nT + \phi) + V_{os} + (-1)^n \frac{\Delta V_{os}}{2} \tag{3}
\]

Using \((-1)^n = \cos(\omega_0 nT / 2)\), (3) can be written as

\[
y[n] = \cos(\omega_0 nT + \phi) + V_{os} + \frac{\Delta V_{os}}{2} \cos(\omega_0 nT / 2) \tag{4}
\]

The second and third terms in expressions (4) show that different offsets contribute to a dc value and a periodic additive pattern in the output of the ADC array:

\[
f(\text{noise}) = k \star f_s / 2 \quad k = 1, 2, 3... \tag{5}
\]

**B. Gain mismatch effects**

A mathematical analysis of the output of a two-channel time-interleaved ADC with only gain error is given here. Let \( G = 0.5(G_1 + G_2) \) and \( \Delta G = G_1 - G_2 \). The ADC output with input \( x(t) = \cos(\omega_0 t + \phi) \) is

\[
y[n] = G \cos(\omega_0 nT + \phi) + \frac{\Delta G}{2} \cos(\omega_0 - \omega_1 / 2) nT + \phi \tag{6}
\]

In this equation, the first term is the scaled input and the second term is the image of the input due to channel gain mismatch. The last term in (6) shows the image amplitude that is proportional to the gain error \( \Delta G \). Gain mismatches between the parallel channels cause amplitude modulation of the input samples by the sequence of channel gains. In the frequency domain, this error causes a copy of the input signal spectrum to appear centred around the channel sampling rate, \( f_s / 2 \).

**C. Clock timing error effects**

Deviations from the ideal sampling time can be represented as a sequence of sample-time errors that introduce errors in the input samples. For a sinusoidal input, the input samples are phase modulated by the sequence of sample-time errors in the ADC channels. In the frequency domain, this error produces copies of the input signal spectrum at the same frequencies as the spurious components stemming from gain mismatch. In spectral point of view, gain and clock timing errors spurs positions appears in the same way. To make the difference, only the clock timing error decreases the SNR when we increase the input frequency.

**III. THE SIMULINK MODEL**

We decide to use Simulink of Matlab because of the wide range of functionalities and toolboxes which allow to designer flexibility in programming. The detail of blocs shown in Fig. 2 is presented in [3]. In this paper, we will be satisfied to present results of Simulink model.

![Simulink Time Interleaved ADC model](image)

The next figure present output spectrum of two TIADCs channel.

![Gain and offset mismatch effects](image)
The offset and gain mismatch component localization validate formulas of II.A and II.B.

Timing errors are the last errors to be treated in this paper. A sampling system is presented in Fig. 3. To emphasize the jitter effects, we will sample the input signal with the same frequency. The sampling system output is a noise proportional to the slew rate and the jitter value.

This system is validated in Fig. 5 and Fig. 6 by computing the standard deviation of the output.

### IV. THE NEW MODEL

#### A. Necessity

In [3], qualitative and quantitative validation of jitter model is presented to show the influence of this error in spectral parameters. In the qualitative one, we make the magnitude input signal changing until full scale and we compute the SNR of the whole system. After the quantization effects, the SNR is fixed at value corresponding to the formulas given in [1] and [2].

The quantitative validation method is based to spectrum computing with two different jitter values. When jitter value is doubled the noise floor is increased by 6 dB, which correspond to theoretical value.

As disadvantage of the Simulink model, we can say that the validation of this model is functional only with specific values of input jitter. In fact, we have to increase the jitter value, to have suitable results. We were obliged, in previous work, to confound the internal ADC jitter and the test bed jitter (generator noise for example). This assumption is not still true especially when we increase the ADC speed.

A new model will be created to:

- Have a better performance in spectral parameter of the entire ADC system. We have to use a modeling environment with many abstraction levels to be more accurate.
- In order to implement in DSP some compensation algorithms to correct gain, offset and timing mismatch errors. We decide to prepare a material environment for simulations. To be near to the reality in the modeling process we decide to use the VHDL-AMS language. All system described by an in time Differential Algebraic Equation can be described by this language. With this language we will model the sample and hold block, the quantizer and the saturation block to limit the output magnitude to the full scale. The static errors and the jitter effects block detailed in Fig. 1 will be modeled.
- To estimate the nonlinearity function, we will implement a new method proposed in [11]. It consists on an FFT approach to estimate the INL. The big advantage of this method is the requirement of little number of samples with respecting the classic methods. This method will permit to implement fast and inexpensive linearization algorithm to maximize the spurious free dynamic range of A/D converter.

#### B. Simulation

In this part we will expose some simulation results with VHDL-AMS. These results are about the noise jitter block which is the main interest of our work. The static errors are quite easy to be implemented. In the new model we use the same sampling system presented in Fig. 4, [13]. The simulation results are presented in next figure. We validate the model by spectral analysis done in Scilab, [14]. The jitter value is estimated by computing the noise floor in dB/Hz.
\[ \text{PSD}(dB/Hz) = 10\log(2\pi f_c)^2 + 10\log(\sigma^2 / f_{\text{coh}}) \]  

(8)

For \(-117\text{dBc/Hz}\) of noise floor we calculate 113fs as internal jitter. Knowing that, in practice we measure as internal jitter value under 1ps. This model can be in agreement with this range of value. This computation is very useful to justify the necessity to change the model and the modeling approach. Note that with SIMULINK model we are not able to go under 10ps.

**V. CONCLUSION**

A Simulink model of two channel time interleaved ADC has been developed. The speed and the flexibility of this model has been compensated by the lack of accuracy especially when we have to decrease the jitter value. We decide to use VHDL-AMS as language and modeling environment to have more accuracy and to have a material approach. A new INL spectral estimation method will be presented and implemented.

**REFERENCES**


